10/056,935

LOW POWER AUTO-REFRESH CIRCUIT AND METHOD FOR DYNAMIC RANDOM ACCESS MEMORIES

ABSTRACT OF THE DISCLOSURE

A power saving circuit disables input buffers for command and address signals during an auto-refresh of a DRAM. The input buffers are re-enabled at the end of the auto-refresh in a manner that does not cause spurious commands to be generated. The power saving circuit prevents spurious commands by biasing internal command signals to a "no operation" command whenever the input buffers for the command signals are disabled. The DRAM may also be placed in a mode in which it automatically transitions to a low power precharge mode at the end of the auto-refresh to further reduce power consumed by the DRAM.